

Fig. 1A

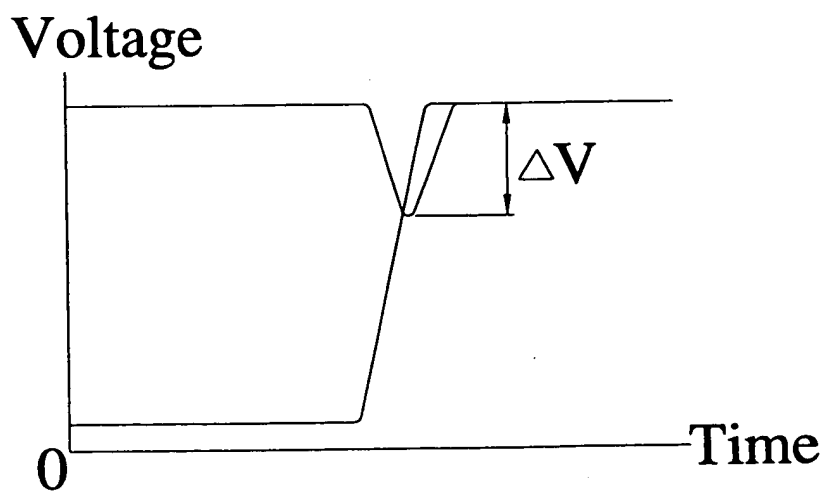


Fig. 1B

A cross-sectional view of a semiconductor device 100. The device features a substrate 160 with a top layer 165 and a bottom layer 167. A central region 150 is defined by dashed lines 170 and 180. This region contains a top layer 125 and a bottom layer 155. A central layer 157 is positioned between the top and bottom layers of the central region. On the left side, a gate structure 110 is shown, with a top gate 105 labeled V+ and a bottom gate 115 labeled V-. The gate structure is connected to a central region 120. On the right side, a gate structure 130 is shown, with a top gate 140 and a bottom gate 135. The central region 150 is connected to the central region 120 on the left and the central region 130 on the right.

Fig. 2A

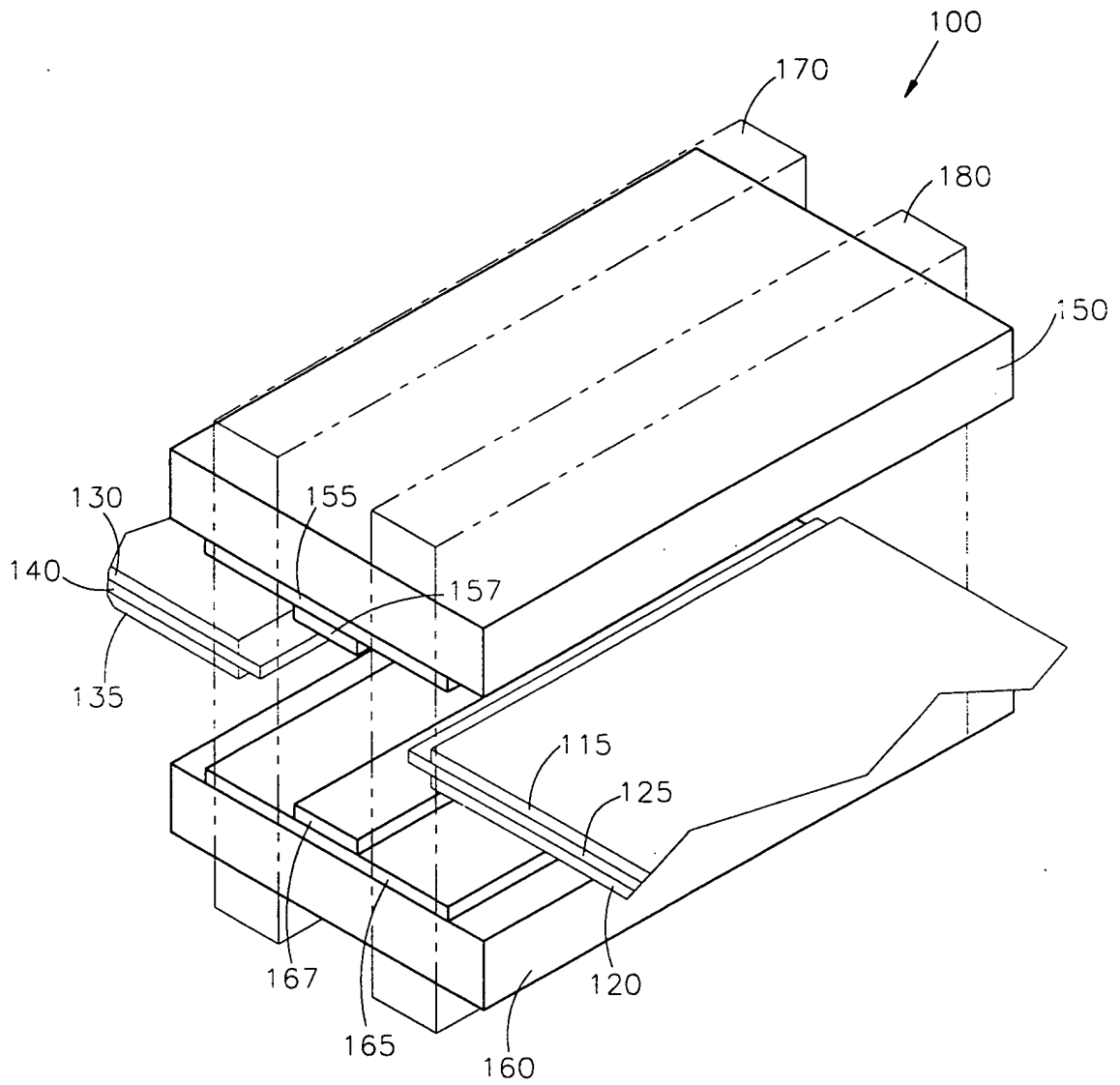


Fig. 2B

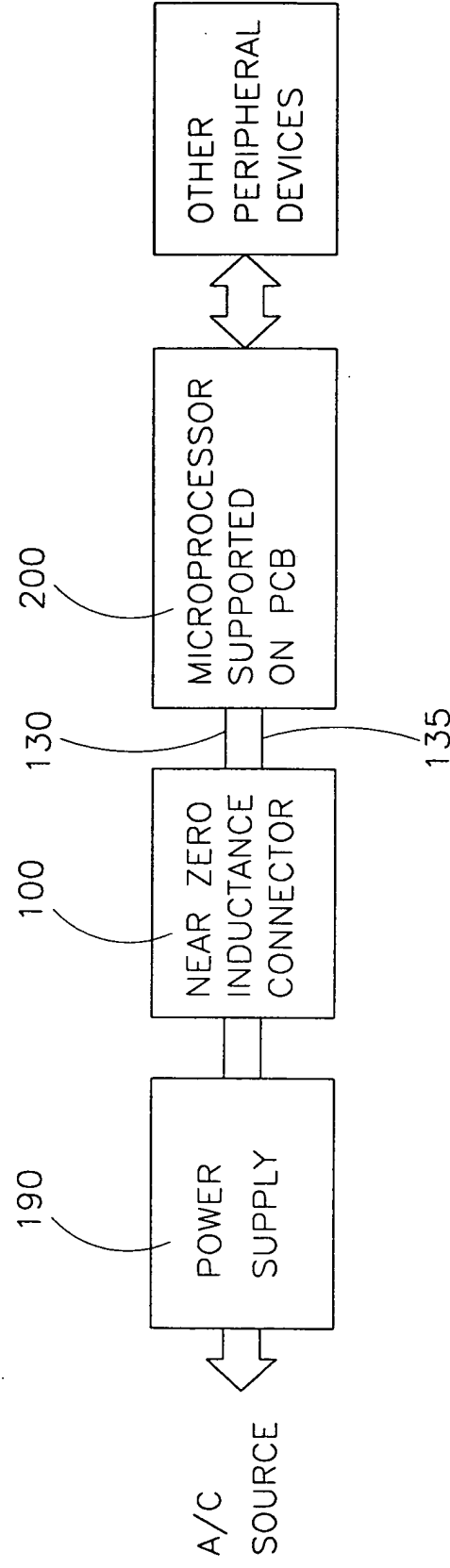


Fig. 3

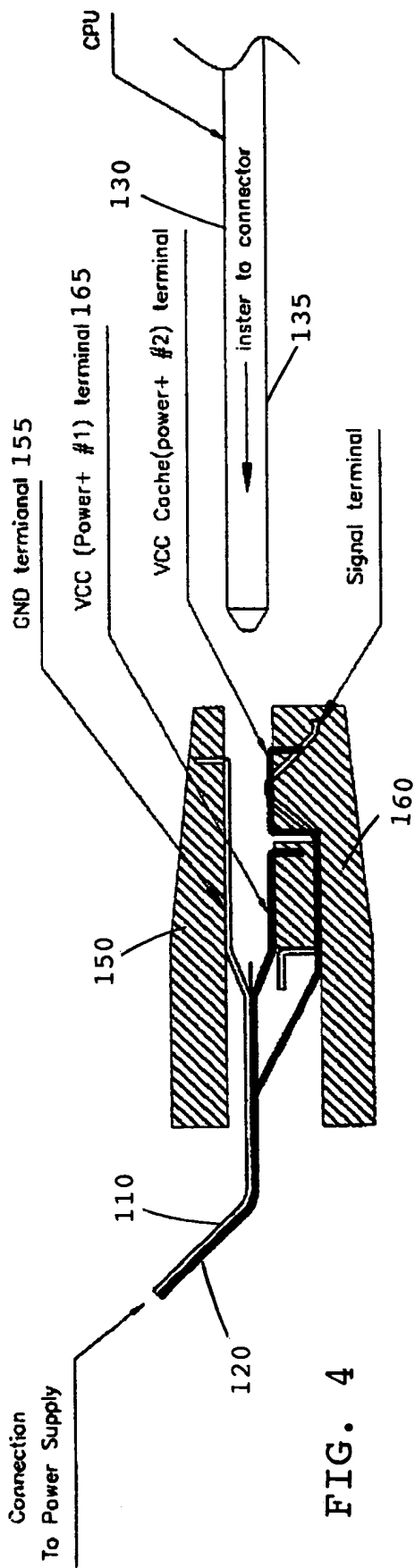


FIG. 4

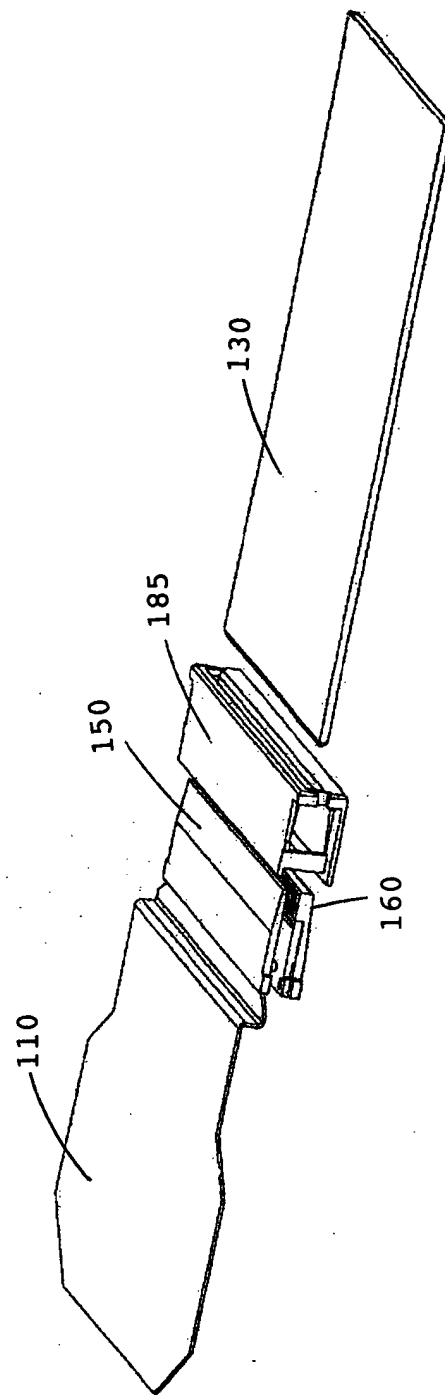


FIG. 5A

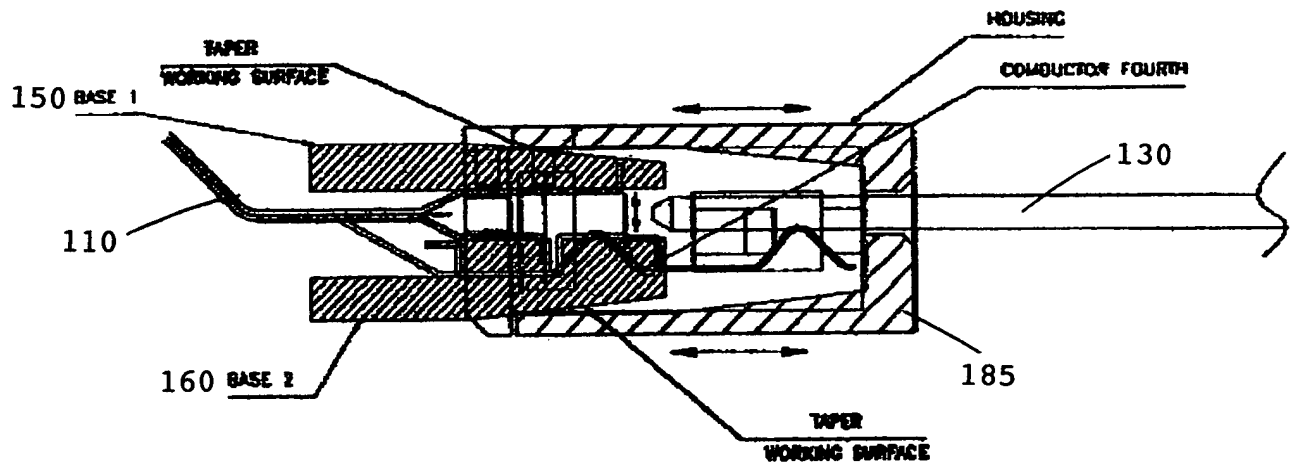


FIG. 5B

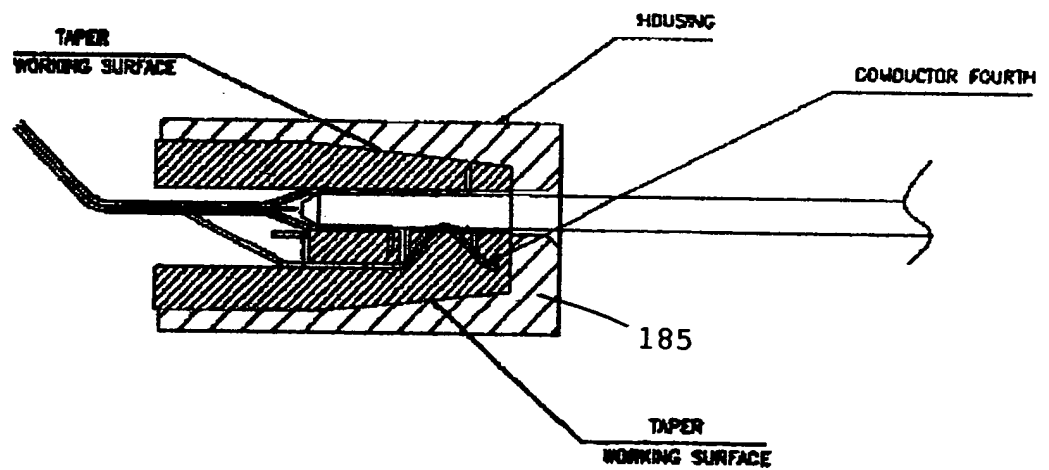


FIG. 5C

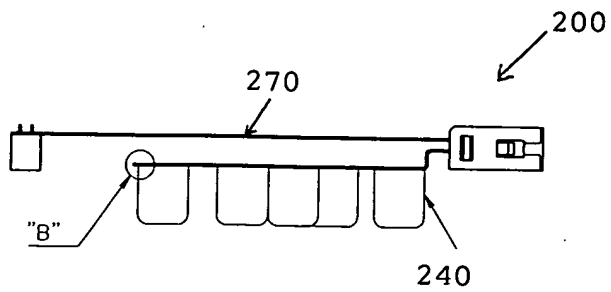


FIG. 6A

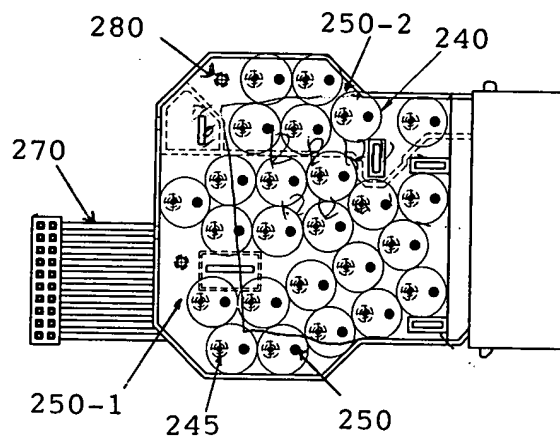


FIG. 6B

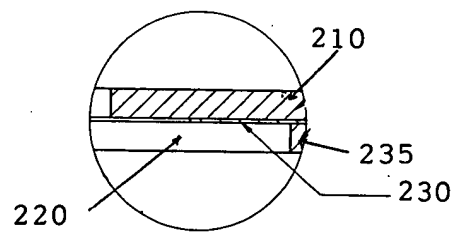


FIG. 6C